ABSTRACT OF THE DISCLOSURE

A programming voltage is applied to a first word line coupled to a control gate of a selected ferroelectric memory cell in an array of ferroelectric memory cells. A gate/source voltage equal to the programming voltage is sufficient to reverse polarity of each memory cell. A ground potential is applied to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell. A fraction of the programming voltage is applied to other word lines coupled to control gates of non-selected memory cells not associated with the first word line, other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line, and other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line.